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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,182	08/28/2003	Jeffrey J. Terlizzi	1400-35	6462

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EXAMINER	
HESS, DANIEL A	
ART UNIT	PAPER NUMBER
2876	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/650,182	TERLIZZI, JEFFREY J.	
	Examiner	Art Unit	
	Daniel A. Hess	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to Applicant's filing of a Request for Continuing Examination (RCE) on 2/5/2007, which has been entered into the electronic file of record.

Oath/Declaration

The Examiner's objection to the Oath is withdrawn. The new Oath meets all requirements.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US 6,705,527) in view of the Wikipedia article 'Flash memory.' It is importantly noted that the Wikipedia article is being used not as a secondary reference, but as a supporting document, providing evidence to support the Examiner's claims about well-known flash memory. Thus, the date of the Wikipedia article is not relied upon. Instead, the technology of flash memory has well-known priority and well-known advantages which are supported by the Wikipedia article.

Re claims 1, 3-5, 7, 8, 10-13, 15, 17-20, 22: Kelly discloses a data acquisition device (a data reading device 10. such as a bar code scanner) for acquiring bar code data (see figure 1)., at least one host device (30a-30n) for receiving and processing the acquired data; and an interface controller for interfacing the data acquisition device to the at least one host device (see figure 2)., said interface controller comprising: a microcomputer 60 for receiving data from the data acquisition device, including the acquired data, and outputting a host device type signal (see figure 2) and interface circuitry 70, 80 in operative communication with the microcomputer 60 for receiving the host device type signal (via based on the different pin signal received) and the data received by the microcomputer 60, selecting at least one interface from a plurality of interfaces in accordance with the host device type signal (see col. 8, lines 10+), and transmitting the received data including the acquired data (decoded bar code data) to at least one host device. The scanner functional block diagram shows (see figure 2) the plurality of drivers 70, 80 for driving output signal to voltage levels acceptable by the at least one host device, and further teaches a multiplexer (shown as an 1/0 multiplexer circuitry in figure 2) as a plurality of switches for coupling host specific outputs from the microcomputer to an output connector of the interface controller by selecting particular interface deriver circuit to be used when sending data signal to the output connector 90 (see col. 5, lines 1+., col. 7, lines 39+*, col. 9, lines 11+., and figure 2). Regarding the limitations of a single circuit board for multiple interfaces, where one of the interfaces is USB see figure 3, which shows the interfaces that are supported, including USB.

Regarding newly added limitations that "the microcomputer includes flash memory storing programmable instructions for enabling configuration of the interface circuitry" the limitation is almost fully met by Kelly et al., with the exception that Kelly et al. is silent on what type of memory is employed. From Kelly's teaching (column 7, lines 50+), some things are clear. Firstly, the interface controller of Kelly et al. is programmable. It is capable of receiving various programming interfaces. Second, the interface controller necessarily and inherently contains a changeable memory (as opposed to hard wiring) because it can receive new protocols.

Flash memory offers several well-known advantages, including durability and low cost. As the Wikipedia article "Flash Memory" points out in the first paragraph "Flash memory costs far less than EEPROM and therefore has become the dominant technology wherever a significant amount of non-volatile, solid-state storage is needed." Further, flash memory long precedes the instant invention, as the Wikipedia article makes clear in the 'History' section, with major developments occurring in the 1980s.

In view of the well-known flash memory, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the old and well-known flash memory as the necessary and inherent memory of Kelly which stores protocol information, with the motivation to of its comparatively low cost.

Re claim 2, 9, 16, 21: While Kelly et al. in general shows hard-wiring rather than modules stored in memory, it is understood in the hard that both approaches are equivalent.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the old and well-known program procedures for converting the data type rather than hard-wiring because programming can be easily updated to add additional formats by loading new software. Hardwiring does not have this benefit.

Re claim 6: In Kelly et al. it is presumed that decoding takes place at the scanner. If the scanner is connected to the interface controller, then they can be seen as a continuous system, and it can be said that the scanner performs decoding, at least to a certain extent.

Re claim 14: In the present case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the scanner and universal connector integral, because in this way one can produce a scanner that is universally connectable.

There is no unexpected result from making integral.

Re claim 24: It is common and typical in the art of computing systems to check ports to confirm that needed peripherals are connected. The motive is simply to detect the common and easily-solved problem of incomplete connections.

Re claim 25: It is clear that one should connect a host-specific output to a particular host device because that is just what it was designed for in Kelly et al.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. in view of the Symbol Product Reference Guide (of record in IDS of 5/22/06).

Selecting an interface type for a barcode scanner by scanning a barcode is shown throughout the LS 2501 Programmer's Guide.

In view of Symbol's teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to input the interface type by allowing the user to scan a barcode because the system already includes a banner and this can keep the scanner design simple by reusing this same input.

Response to Amendment/Arguments

Regarding newly added limitations that "the microcomputer includes flash memory storing programmable instructions for enabling configuration of the interface circuitry" the limitation is almost fully met by Kelly et al., with the exception that Kelly et al. is silent on what type of memory is employed.

Kelly teaches (column 7, lines 50+), "The desired **host interface for the data reader is communicated to the device through any one of various methods**, such as by signals initiated from the interconnect cable itself or by scanning the information from a configuration bar code. The UIDA then **selects the appropriate host interface protocol** and configures the scanner for operation with the host processing device."

From the above, several things are clear. Firstly, the interface controller of Kelly et al. is programmable. It is capable of receiving various programming interfaces. Second, the interface controller contains a changeable memory (as opposed to hard wiring) because it can receive new protocols. Third, there are 'instructions for enabling configuration of the interface circuitry' since the host interface protocol dictates how the interface must be configured. This third point is made more clear at column 8, lines 15+: "Depending on which pin signals are received, the Interface Select Logic Block 210 configures the UIDA 200 to support any of the host interface protocols illustrated in FIGS. 6 through 13."

As for the use of flash memory, one of ordinary skill, when noting that Kelly et al. is silent on what kind of memory is used in the interface controller, would have a strong motivation to use flash memory because of its comparatively low cost. As the Wikipedia article "Flash Memory" points out in the first paragraph "Flash memory costs far less than EEPROM and therefore has become the dominant technology wherever a significant amount of non-volatile, solid-state storage is needed."

Regarding the amendment in claim 20 including the limitation that the interface controller performs 'translating' functions, this is indeed the very essence of Kelly et al. Kelly et al. receives a signal and is capable of translating it into any one of a variety of protocols. Figure 3 shows eight different modes that are supported. There is therefore support for translation into any of these modes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel A. Hess whose telephone number is (571) 272-2392. The examiner can normally be reached on 8:00 AM - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel A Hess
Examiner
Art Unit 2876

3/17/07